



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/102,207	06/22/1998	DAVE GOH	10971798-1	1530
22879	7590	05/14/2004	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			DAVIS, DAVID DONALD	
			ART UNIT	PAPER NUMBER
			2652	
DATE MAILED: 05/14/2004				

20

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/102,207	GOH ET AL.
Examiner	Art Unit	
David D. Davis	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 February 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) 31-41 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-30 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- | | |
|--|--|
| 15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 17) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. | 20) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. In view of the newly discovered reference to Cromer et al (US 6,532,4997) and the Appeal Brief filed on February 27, 2004, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
 - (2) request reinstatement of the appeal.
2. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Election/Restrictions

3. Claims 31-41 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 10, received November 15, 2001.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5, 6, 8, 12-15 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cromer et al (US 6,532,497). As per claim 1, Cromer et al shows in figure 4 and describes in column 3, lines 32-52 a chip 300 for incorporation within a network device connectable to a computer network. The network device includes a host processor 200 and the chip 300 including a media access controller 308 connectable to the computer network. The media access controller 308 providing the chip 300 with access to the computer network independent of the host processor 200.

Figure 4 of Cromer et al also shows a host interface connectable to the host processor 200 and an embedded processor 400 coupled between the host interface and the media access controller 308. Cromer et al discloses in column 3, lines 32-52 that the embedded processor 400 is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor 400 further is programmable to send the manageability information to the media access controller 308 for transmission over the computer network. The chip 300, as described in column 3, lines 32-52, performs network management functions independent of the host processor 200.

As per claim 2, the embedded processor 400 of chip 300 is programmable to obtain the manageability information in response to a network request addressed to the manageability web server, as described in column 3, lines 32-52. As per claim 3, the network device, as shown in figure 4, further includes an interchip communications and a compliant device coupled to the interchip communication. The chip 300 includes an interface connectable to the interchip

communications. The embedded processor 400 is programmable to communicate via the interchip communication interface to obtain manageability information about the compliant device, as described in column 3, lines 32-52.

As per claim 5, Cromer et al shows in figures 4-5 and describes column 3, line 32 through column 4, line 5 that the embedded processor 400 is also programmable to control the compliant device coupled to the interchip communications. As per claim 6, Cromer et al Cromer et al shows in figures 4-5 and describes column 3, line 32 through column 4, line 5 that the compliant device is a power supply controller and the embedded processor 400 is programmable to control the power supply controller. As per claim 8, Cromer et al shows in figures 4-5 and describes column 3, line 32 through column 4, line 5 that the embedded processor 400 is programmable to control the compliant device in response to a network request addressed to the manageability web server. As per claim 12, Cromer et al shows in figures 4-5 and describes column 3, line 32 through column 4, line 5 that the embedded processor 400 is programmable to obtain manageability information from the host processor 200.

As per claim 13, Cromer et al shows in figures 4 and 5 and describes in column 3, line 32-5 a network device connectable to a computer network. The network device including interchip communications; a compliant device coupled to the interchip communications; a chip 300 including a media access controller 308 connectable to the computer network; an interchip communications interface connected to the interchip communications and an embedded processor 400 coupled to the interchip communications interface and the media access controller 308.

Figure 5, in particular, of Cromer et al shows non-volatile memory programmed with a plurality of executable instructions (source, destination, length, etc.). The instructions, when executed, instructing the embedded processor 400 to function as a manageability web server, communicate with the interchip communications to obtain manageability information about the compliant device and send the manageability information to the media access controller 308 for transmission over the computer network.

As per claim 14, the instructions instruct the embedded processor 400 to obtain the manageability information from the compliant device in response to network requests addressed to the manageability web server. As per claim 15, Cromer et al shows in figure 4 a host processor 200. The chip 300 includes a host interface coupled to the host processor 200 and the embedded processor 400, and the instructions instruct the embedded processor 400 to obtain manageability information from the host processor 200.

As per claim 19, Cromer et al shows in figure 5 and discloses in column 3, line 37 through column 4, line 5 the non-volatile memory further stores web page content. As per claim 20, Cromer et al also shows in figure 5 and describes in column 3, line 53 through column 4, line 5 that volatile memory 504 is for storing the manageability information.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102((e), f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 7, 9-11, 18, and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cromer et al (US 6,532,497). As per claim 23, Cromer et al shows in figure 4 and describes in column 3, lines 32-52 a system including a computer network; a network device including a host processor 200 and a chip 300. Cromer et al shows in figures 4 and 5 the chip 300 including a media access controller 308 coupled to the computer network and an embedded processor 400 coupled to the media access controller 308.

In column 1, lines 40-44 of Cromer et al discloses that processor 400 can be programmed to function as a manageability web server and a network manager coupled to the computer network. Cromer et al shows in figures 4 and 5 and describes in column 3, lines 32-52 that the embedded processor 400 can communicate with the network 14 manager independent of the host processor 200.

As per claim 24, Cromer et al shows in figure 4 and describes column 1, lines 40-44 the network device including a compliant device and with the embedded processor 400 programmable to control the compliant device in response to control requests from the network

manager. As per claims 26 and 27, Cromer et al discloses in column 3, lines 15-23 that the compliant device is a power supply controller. The network manager can request the embedded processor 400 to control the power supply controller to shut down, to reboot and turn on the network device at scheduled times.

As per claim 29, Cromer et al discloses column 1, lines 40-43 that the network manager can send a diagnostic program to the embedded processor 400 and request the embedded processor 400 to run the diagnostic program and return to the network manager results obtained by the diagnostic program. As per claim 30, Cromer et al discloses in columns 3, lines 37-52 that the embedded processor is programmable to communicate with host interface and obtain manageability information from the host processor 200 in response to requests by the network manager.

Cromer et al, however, is silent as to the network manager including a web browser and a plurality of HTML files for instructing the network manager to communicate with the embedded processor in the network device and perform network management of the network device. Cromer et al, however, is also silent as the embedded processor controller a fan and performing firmware/BIOS program upgrades. Cromer et al is additionally silent as to the embedded processor utilizing TCP/IP, acting as an *HTTP* web server.

Official notice is taken of the fact that web browsers; HTML files; TCP/IP protocols and HTTP web servers for networks are notoriously old and well known in the art. Official notice is also taken of the fact that fans and programs to perform firmware/BIOS upgrades are notoriously old and well known in the computer art.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to utilize known and commonly used network software, files, protocols and servers as taught in the network art in the network system of Crommer et al. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to utilize known and commonly used network software, files, protocols and servers as taught in the network art so that a networking system is able to integrate and communicate with existing servers and clients in the network.

It also would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide network system of Crommer et al to control a fan and perform upgrades as taught in the art. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to allow a network to control a fan and perform upgrades, which is well within the purview of a skilled artisan and absent an unobvious result, so that a system is able to be cooled and updated remotely.

9. Claims 4, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cromer et al (US 6,532,497) in view of Han (US 5,903,737). Cromer et al discloses the claimed invention. However, Cromer et al is silent as to the interchip communications including an I²C bus with the compliant device being an I²C-compliant device.

Han discloses in column 2, lines 58-67 I²C serial data communications.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide the device of Cromer et al with I²C serial data communications as taught by Ham. The rationale is as follows: one of ordinary skill in the art at the time the

invention was made would have been motivated to provide I²C serial data communications so as to provide an apparatus "which can transmit and receive serial data of an inter integrated circuit (IIC or I²C) type utilizing a general microcomputer." See column 1, lines 6-12 of Han.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David D. Davis whose telephone number is (703) 308-1503. The examiner can normally be reached on Monday thru Friday between 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T. Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David D. Davis
Primary Examiner
Art Unit 2652

ddd